P27154.D01 Serial No. 10/708,430

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of:	Docket No. P27154
Michael P. Belyansky, *et al.*	Confirmation No. 2429
Appln. No. : 10/708,430	Group Art Unit: 2818
Filed : March 3, 2004	Examiner: A. Huynh
For : MOBILITY ENHANCED CMOS DEVICES	

Commissioner for Patents
U.S. Patent and Trademark Office
Customer Service Window, Mail Stop Amendment
Randolph Building
401 Dulany Street
Alexandria VA 22314

DECLARATION UNDER 37 C.F.R. 1.131

Sir:

We, Bruce B. DORIS, Oleg G. GLUSCHENKOV, and Michael P. BELYANSKY do hereby declare:

1. We are co-inventors of the subject matter disclosed and recited in independent claims 1, 19 and 31 of the above-identified application.

2. We completed the invention of claims 1, 19 and 31 (and those claims dependent thereon) in the United States before July 25, 2003, as evidenced below.

CONCEPTION

3. Before July 25, 2003, we conceived of a method of manufacturing a semiconductor structure, comprising the steps of forming spacer voids between a gate a mandrel layer, creating recesses in a substrate below and in alignment with the spacer voids, filling a first portion of the recesses with a stress imposing material, filling a second portion of the recesses with a semiconductor material, and removing the mandrel layer before July 25, 2003.

4. We also conceived of a method of manufacturing a semiconductor structure, comprising the steps of forming dummy spacers on sides of a gate formed on a substrate, forming a mandrel layer with portions of the mandrel layer abutting the dummy spacers, removing the dummy spacers to form spacer voids between the gate and the mandrel layer, creating recesses in the substrate below and in alignment with the spacer voids, filling a first portion of the recesses with a stress imposing material, and filling a second portion of the recesses with a semiconductor material before July 25, 2003.

5. We also conceived of a method of manufacturing a semiconductor structure, comprising the steps of forming a field effect transistor gate on a substrate, forming a first dummy spacer and a second dummy spacer on sides of the field effect transistor gate, forming a mandrel layer with portions of the mandrel layer abutting the first and second dummy spacers for the field effect transistor gate, after masking the semiconductor, introducing stress to the field effect transistor gate, and removing the mandrel layer, wherein the step of introducing stress material comprises removing the first and second dummy spacers from the field effect transistor gate to form first and second spacer voids between the field effect transistor gate and the portions of the mandrel layer, creating a first recess in the substrate below and in alignment with the first spacer void and a second recess in the substrate below and in alignment with the second spacer void for the field effect transistor gate, filling a first portion of the first recess and a first portion of the second recess with a stress imposing material configured to enhance performance of the field effect transistor gate, filling a second portion of the first recess and a second portion of the second recess for the field effect transistor gate with a semiconductor material, and unmasking the semiconductor structure before July 25, 2003.

6. Evidence of such conceptions as disclosed and recited in claims 1, 19 and 31 of the application is shown in an embodiment of which is evidenced by IBM Invention Disclosure FIS8-2003-0281 (hereinafter referred to as "the Invention Disclosure") attached hereto as Exhibit A. The Invention Disclosure attached hereto is a

photocopy of and are identical to the originals, except that all pertinent dates have been removed therefrom.

7. All relevant dates removed from the Invention Disclosure and other attached documents attached hereto are before July 25, 2003.

8. The benefits and features of the recited invention are shown and described in the Invention Disclosure and accompanying documents.

9. These features and others are exemplified in the figures accompanying the Invention Disclosure.

DUE DILIGENCE

10. At least inventor Bruce B. DORIS communicated with outside patent counsel, Andrew M. Calderon, in preparing a patent application based on the Invention Disclosure.

11. We worked diligently on the preparation of the patent application by first submitting the Invention Disclosure statement to in-house IBM counsel. In particular: on or about May 27, 2003, the invention disclosure FIS8-2003-0281 was opened; on or about May 29, 2003, this invention disclosure was sent to an IBM evaluator; on or about May 29, 2003, this invention disclosure was evaluated; and on or about July 11, 2003, the invention disclosure was reviewed.

12. After a prior art search was conducted and the Invention Disclosure was mailed to outside counsel, Andrew M. Calderon, we worked diligently on the preparation of the patent application with outside patent counsel Andrew M. Calderon until a final draft patent application was completed to our satisfaction. Communications took place between at least one of the Inventors and Mr. Calderon at least between July 11, 2003 and February 4, 2004.

13. A final draft of the patent application was forwarded to IBM in-house counsel on February 4, 2004 for execution of the formal documents by all of the inventors. The inventors signed the documents for filing in the U.S. Patent and Trademark Office, which was effectuated on March 3, 2004 by in-house counsel.

14. We declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further, that the statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Bruce B. DORIS	Date
Oleg O. GLUSCHENKOV O.G.	12/14/2005 Date
Michael P. BELYANSKY	12/16/2005 Date

Disclosure FIS8-2003-0281

Prepared for and/or by an IBM Attorney - IBM Confidential

Created By Bruce Doris On
Last Modified By Oleg Gluschenkov On

Required fields are marked with the asterisk (*) and must be filled in to complete the form.

***Title of disclosure (in English)**
MOBILITY ENHANCED CMOS DEVICES

Summary

Status		Under Evaluation
Final Deadline		
Final Deadline Reason		
*Processing Location		Fishkill
*Functional Area	select	(KBG) KBG ... CHEN: CMOS-6X/HPLS
Attorney/Patent Professional		Joseph P Abate/Fishkill/IBM
IDT Team	select	Oleg Gluschenkov/Fishkill/IBM William Devine/Fishkill/IBM DOMINIC SCHEPIS/Fishkill/IBM David Hanson/Fishkill/IBM Thomas Dyer/Fishkill/IBM Noah Zamdmer/Fishkill/IBM DURESETI CHIDAMBARRAO/Fishkill/IBM Werner Rausch/Fishkill/IBM
Submitted Date		
*Owning Division	select	MD
Incentive Program		
Lab		
*Technology Code		101N2
PVT Score		

Inventors with a Blue Pages entry

Inventors: Bruce Doris/Fishkill/IBM, Oleg Gluschenkov/Fishkill/IBM, Michael P Belyansky/Fishkill/IBM

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> denotes primary contact

Inventors without a Blue Pages entry

IDT Selection

Attorney/Patent Professional	Joseph P Abate/Fishkill/IBM
IDT Team	Oleg Gluschenkov/Fishkill/IBM William Devine/Fishkill/IBM DOMINIC SCHEPIS/Fishkill/IBM David Hanson/Fishkill/IBM Thomas Dyer/Fishkill/IBM Noah Zamdmer/Fishkill/IBM DURESETI CHIDAMBARRAO/Fishkill/IBM Werner Rausch/Fishkill/IBM
Response Due to IP&L	

***Main Idea**

1. Background: What is the problem solved by your invention? Describe known solutions to this problem (if any). What are the drawbacks of such known solutions, or why is an additional solution required? Cite any relevant technical documents or references.

Mobility enhanced devices are likely to enable the continued performance trend for high performance ligic circuits. Several approaches to generate mobility improvements are actively being persued. One approach is to strain the Si by growing epitaxy Si on relaxed SiGe layers. This, traditional approach has several drawbacks. Specifically, no pFET improvement has been observed for Ge concentrations below 30%. In addition, the technique is capable of generating a significantly high density of defects. Dopant diffusion of Arsenic is also problematic in SiGe layers and can lead to degraded short channel effects.

Alternate approaches to improving mobility in short channel devices is gaining a great deal of attention. Local mechanical stress is capable of enhancing mobility in both nFETs and pFETs. In addition, the process and device related problems associated with strained Si by SiGe are overcome by the local mechanical stress approach.

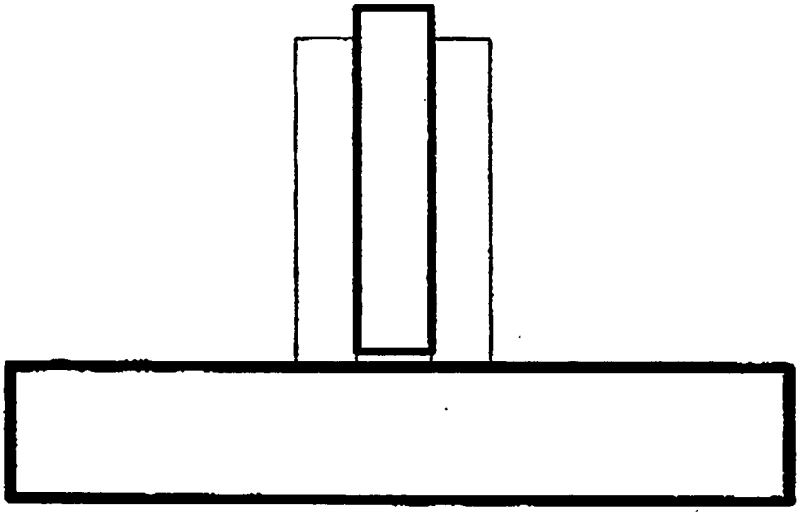
This invention is directed toward stress enhanced cmos devices. The invention has unique structure and method to achieve the structure which results in significant device performance improvement for both pFETs and nFETs.

2. Summary of Invention: Briefly describe the core idea of your invention (saving the details for questions #3 below). Describe the advantage(s) of using your invention instead of the known solutions described above.

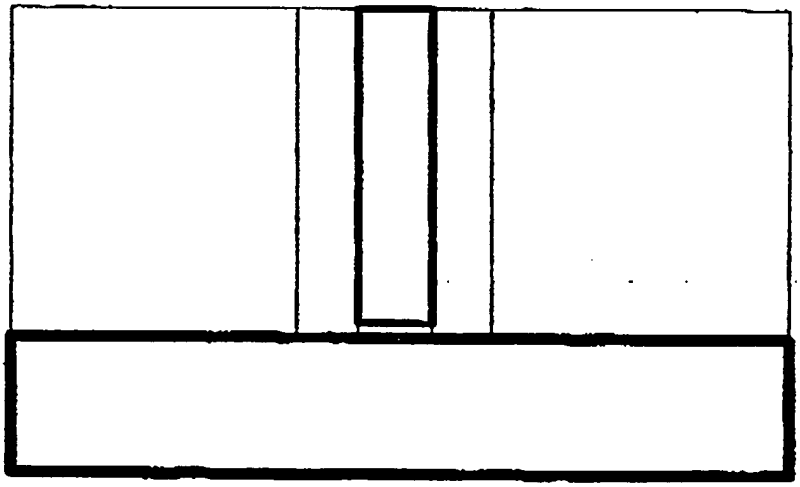
A standard process flow is used to fabricate the structure shown below. A typical sequence may include but is not limited to first providing a semiconductor substrate. Next, an isolation shceme is used to isolate devices. The isolation shceme may be a measa type isolation shceme, local oxidation of Si (LOCOS) scheme or a shallow trench isolation scheme. Well implants are used to set threshold voltages. A gate oxidation process is next carried out followed by gate patterning. In one embodiment, a hard mask is left ontop of the gate electrode after the gate stack etch. After this, a dummy spacer is fabricated by depositing a disposible material and performing a spacer etch. In another embodiment in which the gate cap is used, a thin SiO2 liner is deposited followed by deposition of a poly Si film. A spacer is formed from the poly Si film. Next a dielectric film is deposited and planarized to the top of the gate cap. A block mask is now patterned over the pFET regions. The disposible spacer is then removed from the nFET regions using a wet or dry etch process. If an SiO2 liner is used, then the liner is removed by a wet or dry etch process. Next the Si is etch using a timed etch process. The block mask is now removed. At this point in the process flow, an interfacial layer is fabricated. For example, a nitrided interface as is used in the buried strap process is used. A tensile material is deposited and recessed in the opening. Alternatively, poly SI is deposited and recessed in the hole. Upon annealing, the poly Si grains grow and the material undergoes

a volume contraction. This causes tension in the nFET channel thereby enhancing electron mobility. A similar process sequence may be used to create compression in the pFET channel. One possible choice of compressive material for the pFET is SiGe. Alternatively, dielectric films may be used to stress the channels. After the stressing material is deposited and recessed, a selective epitaxial Si growth process is carried out. The planarized dielectric film is removed selectively with respect to the gate and Si substrate. A standard process flow is used to complete the device build including halo and extension implants, source-drain spacer, source drain implants RTA and silicide formation.

Starting structure with patterned gate and disposible spacer:

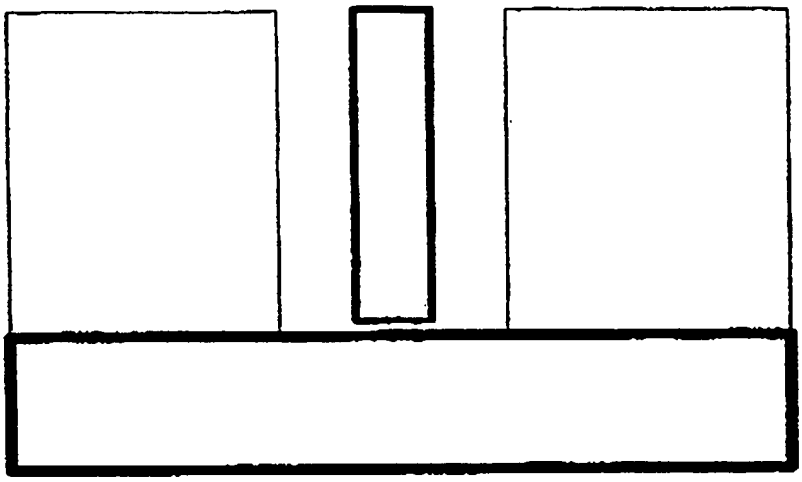


Deposit dielectric film and planarize to top of gate.

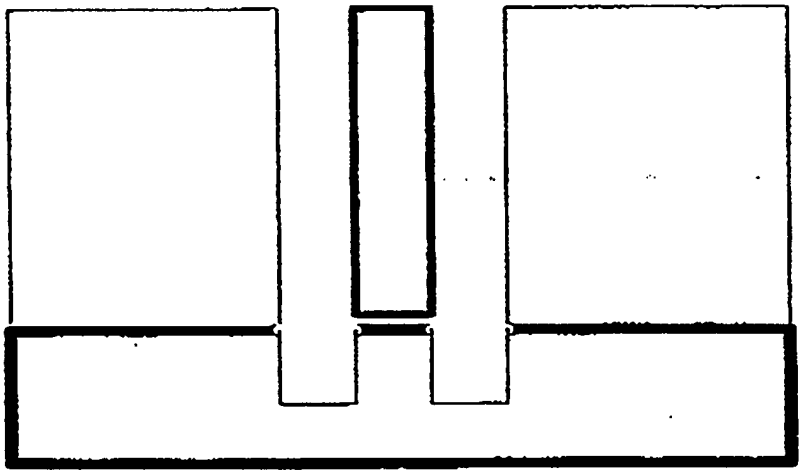


Remove disposible spacer.

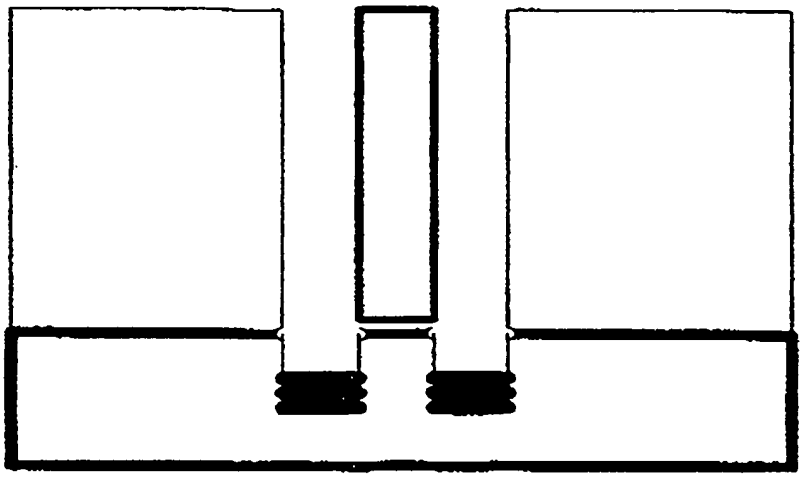
FIS8-2003-0281 MOBILITY ENHANCED CMOS DEVICES - continued



Si recess:



Fill with compressive material for pFET or tensile material for nFET, and recess.



Selectice epitaxial growth: